## REMARKS

Claims 1-23 are pending, with claims 1, 8, 12, 22, and 23 being in independent form. Claims 8, 9, 12, 19, and 23 are amended.

At the outset, Applicant acknowledges with appreciation the Examiner's reconsideration and withdrawal of the rejections raised in the First Office Action.

In the Second Office Action, claims 1, 6, 7, and 22 are rejected for anticipation by U.S. Patent No. 5,457,391 to Shimizu et al. ("Shimizu I"). Claims 8, 9, and 23 are rejected for anticipation by U.S. Patent No. 5,592,097 to Shimizu et al. ("Shimizu II"). Also, claims 8-11 and 23 have been rejected for anticipation by U.S. Patent No. 5,434,717 to Yoshinaga et al. ("Yoshinaga"). Claims 2 and 13 are rejected for obviousness over Shimizu I in view of U.S. Patent No. 5,276,644 to Pascucci et al. ("Pascucci"), and claims 3-5, 12, and 14-21 have been rejected for obviousness over Shimizu I. Applicant believes the pending claims are allowable over the cited documents for the following reasons.

Anticipation requires that every feature of the claimed invention be shown in a single prior document. In re Paulsen, 30 F.3d 1475 (Fed. Cir. 1994); In re Robertson, 169 F.3d 743 (Fed. Cir. 1999). The pending claims positively recite features that are not described in the cited documents.

For example, claim 1 recites, among other things, first and second current mirrors that produce respective first and second currents proportional to at least a portion of the write current that flows in respective first and second directions into respective first and second write head terminals of the write driver. Related method claim 22 recites, among other things, generating first and second currents proportional to at least a portion of the write current that flows in respective first and second directions into respective first and second write head terminals of the write driver. The Examiner asserts that Shimizu I describes first and second current mirrors 10, 11 that produce respective first and second currents $I_1$, $I_2$ proportional to the write current in conjunction with circuit shown in FIG. 5. Applicant respectfully disagrees.

Persons skilled in the art will understand the elements 10 and 11 shown in FIG. 5 of Shimizu I are not current mirrors as the Examiner asserts, but instead are independent constant current sources. Moreover, the skilled artisan will understand that the currents generated by such current sources are fixed, and thus cannot

produce a current that is proportional a time-varying current, such as the write current recited in claims 1 and 22. Shimizu's independent current sources 10, 11, generate constant currents $I_1$, $I_2$ that are used to bias the emitter-follower output stages consisting of Q5, R1 and Q6, R2, respectively.

In contrast, a current mirror, such as that comprising transistors Q6 and Q8 shown in FIG. 2 of this application, can generate a current, e.g., the current flowing in Q8, that is proportional to the write current, e.g., the current flowing into the write head terminal, e.g., Wrp. Accordingly, claims 1 and 22 are believed to be allowable over Shimizu I for at least the above reasons.

Claim 8 is amended to define an arrangement for detecting an open-circuit condition at at least one of a pair of write head terminals of a write driver, the write driver producing a write current that, when passed in at least one of two directions through an inductive head assembly coupled to the pair of write head terminals, polarizes the inductive head according to the at least one direction of the write current. Claim 8 recites, among other things, a current mirror that produces a mirrored write current that is proportional to the write current that is passed through the inductive head assembly in the two directions.

Similarly, method claim 23 is amended to recite, among other things, generating a mirrored write current that is proportional to the write current that is passed through the inductive head assembly in the two directions. Support for the amendments may be found throughout the application, and in particular in paragraphs [0058] through [0062] of the specification and in FIG. 2. No new matter has been added.

Shimizu II, relied upon in the Second Action to reject claims 8 and 23, does not describe a current mirror that generates a mirrored write current that is proportional to the write current that is passed through the inductive head assembly in the two directions. Instead, the current mirror Q1/Q15 shown in FIG. 8 of Shimizu II produces a current IC15 proportional to the current IC1 passed through the inductor LH and resistor RH in only one direction from terminal 4 to terminal 6. Current passed in the other direction, e.g., from terminal 6 to terminal 4 through Q3 and Q2, does not pass through any current mirror. Applicant notes neither the current element 9, nor either of the switching transistors Q3 or Q2, is a current mirror.

Yoshinaga, also relied upon in the Second Action to reject claims 8 and 23, does not describe an open-circuit detection device responsive to the mirrored write current, as required by claim 8. The Examiner asserts that Yoshinaga describes a current mirror, including elements Q18, CM, that produces a mirrored write current, and an open-circuit detection device OPC in FIG. 2. Assuming, only for purposes here, that this is true, it is clear that the OPC detection device of FIG. 2 is not responsive to any mirrored write current that may be produced by transistor Q18 and the current mirror CM. There is no connection shown in the figure. Instead, the OPC detection device is connected and responsive to the head terminal voltages, $V_X$, $V_Y$.

Moreover, each of the write current, set by the transistor Q14 and the control signal VIW (see col. 13; ll. 48-49), the current branched (not mirrored) from the write current, set by transistor Q18 and the control signal VIW, and the current produced by the current mirror CM are constant currents. Accordingly, the OPC detection device cannot be responsive to any of these currents, as they do not change when an open-circuit condition occurs. Thus, claim 8 is believed to be allowable for at least this reason.

Yoshinaga also does not describe detecting an open-circuit condition at at least one of the first and second write head terminals when the magnitude of the write current drops below a predetermined value, as now required by claims 8 and 23. The Action asserts that Yoshinaga describes a current mirror Q18, CM and an open-circuit detection device OPC that detects and open-circuit condition when magnitude of the mirrored write drops below a predetermined value, but the assertion is incorrect.

Instead, Yoshinaga, describes that if "the magnetic head 5 falls into an open-circuit state, an output voltage from a write driver (WD) is detected to form a signal at low level". Col. 15, ll. 58-61 (emphasis added). In addition, Yoshinaga, in conjunction with the OPC detection circuit shown in FIG. 7, describes at col. 18, ll. 23-33, that:

> When the head is in open state, the head terminals VX, VY are alternately switched corresponding to an output voltage of the write amplifier. Therefore, the opened head cannot be detected by the timer circuit. However, since the voltage at the head terminal VX or VY becomes higher than the reference voltage REF4 corresponding to the

output voltage of the write amplifier, the transistor Q71 or Q72 is turned on to cause a current to flow through the resistor R71 for forming the detecting signal VOS. Thus, the detecting signal VOS at low level is outputted. (emphasis added).

Thus, Yoshinaga, does not describe detecting an open-circuit condition when magnitude of the mirrored write drops below a predetermined value, as required by claims 8 and 23, but instead describes detecting an open-circuit condition based on an output voltage from a write driver. Accordingly, these claims are considered allowable for this reason as well.

With respect to independent claim 12. This claim combines some of the features of claims 1 and 8 to form a novel voltage-mode write driver that is believed to be allowable for at least the same reasons discussed above. Moreover, the remaining dependent claims are considered allowable for these reasons as well.

For the foregoing reasons, Applicant believes the application is in condition for allowance and respectfully requests a Notice thereof at an early date. If any questions remain, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,

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